

WHAT IS CLAIMED IS:

Sub 1. A data processor comprising:
 a CPU for outputting a first address;
 address translation means for inputting said first address,
 5 translating said first address to a second address, and
 outputting said second address; and

address output means for inputting said second address and
 outputting said second address to an external device,

wherein said address translation means stores an external
 10 device control information for controlling said external device
 in association with at least either one of said first address
 or said second address, and outputs said external device control
 information to said external device via said address outputting
 means.

2. A data processor according to claim 1, wherein said
 external device is a device having a PCMCIA interface, and said
 external device control information is an information which
 specifies at least one of an access timing, a memory attribute,
 20 and a bus width of said device having a PCMCIA interface.

3. A data processor according to claim 2, wherein said address
 output means has a timing controller and a bus width and memory
 attribute decider.

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4. A data processor according to claims 2 or 3, wherein said CPU, said address translation means, said address output means, and said PCMCIA interface in said external device are formed on the same semiconductor substrate.

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5. A data processor according to any one of claims 1 to 4, wherein said second address outputted from said address output means is inputted to said address output means via a cache memory and a bus.

6. A data processor according to any one of claims 1 to 5, wherein the control information except for an address is not included in said first address.

7. A data processing system comprising:

a first address for being outputted by a CPU;
address translation means for translating said first address to a second address; and
address output means for outputting an address to both a first external device and a second external device,

wherein when said first address is outputted to said first external device via said address output means, said address output means outputs first external device control information stored in said address output means in association with said first address, together with said first address to said first

external device and

when said second address is outputted to said second external device via said address output means, said address output means outputs second external device control information stored in said address translation means in association with either said first address or said second address, together with said second address to said second external device.

8. A data processing system according to claim 7, wherein said second external device is a device having a PCMCIA interface.

9. A data processing system according to claim 8, wherein said second external device control information includes an information which specifies at least one of an access timing, a memory attribute, and a bus width of said device.

10. A data processing system according to claims 8 or 9, wherein said address translation means outputs said second address and said second address is inputted to said address output means via a cache memory and a bus.

11. A data processing system according to any one of claims 8 to 10, wherein said second external device has a memory or a modem, and said memory or said modem are controlled by said PCMCIA interface controlled by said second external device

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control information.

12. A data processing system according to any one of claims 8 to 11, wherein said CPU, said address translation means, said address output means, and a PCMCIA interface portion in said second external device are formed on the same semiconductor substrate.

13. A data processor connected with a device having a PCMCIA interface via a bus, wherein the control information of said device is stored in a TLB provided in said data processor.

14. A data processing system comprising:
a data processor connected via a system bus; and
a device having a PCMCIA interface,
wherein said data processor keeps the control information of said device in an address translation buffer provided in said data processor, translates an address necessary to access said device by said address translation buffer at the time of accessing said device, and controls said device in accordance with said control information kept in said address translation buffer.

15. A data processor comprising:
a CPU for outputting a first address;

address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

address output means for inputting said second address and outputting said second address to an external device having a PCMCIA interface,

wherein said address translation means stores an external device control information for controlling said external device in association with at least either one of said first address or said second address,

when said first address is inputted to said address translation means, said address translation means outputs said external device control information to said address output means based on said first address or said second address translated based on said first address, and

said address output means outputs said external device control information to said external device.

16. A data processor according to claim 15, wherein said external device control information includes an information which specifies at least one of an access timing, a memory attribute, or a bus width of a device having said PCMCIA interface.

17. A data processor according to claims 15 or 16, wherein said

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